Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended) A method comprising:

determining whether execution of an instruction of a first thread executed in a processor potentially causes a long latency based on whether the instruction hits in a lookup table in an instruction decoder of the processor, the lookup table including entries corresponding to predetermined conditions;

preparing to switch to a second thread based on the determination by selecting a program counter of the second thread within an instruction fetch unit of the processor to fetch a next instruction of the second thread, and executing at least one additional instruction in the first thread present in a pipeline of the processor and storing a result of the at least one additional instruction in a destination storage instead of flushing the at least one addition instruction while preparing to switch to the second thread; and

switching to [[a]] the second thread if the potential long latency is determined ~~based on the determination~~, executing one or more instructions of the second thread in the processor, and storing a result of the one or more instructions of the second thread in the processor.

Claim 2 (cancel)

Claim 3 (previously presented) The method of claim 1, wherein the determining is based on a stochastic modeling of whether the instruction will result in a long latency.

Claim 4 (cancel)

Claim 5 (currently amended) The method of claim [[4]] 1, further comprising providing a feedback signal from the instruction decoder to [[an]] the instruction fetch unit to switch to the second thread if the instruction matches an entry in the lookup table.

Claim 6 (original) The method of claim 1, wherein the long latency comprises less than ten processor cycles.

Claim 7 (canceled)

Claims 8 – 16 (cancel)

Claim 17 (currently amended) An apparatus comprising:

a processor including a processor pipeline having a plurality of pipeline stages to receive and execute instructions, the processor pipeline having a feedback loop coupled between a first pipeline stage and a second pipeline stage to provide a feedback signal generated in the second pipeline stage back to the first pipeline stage to cause the processor pipeline to switch from a first thread to a second thread, the feedback signal to originate from a location in the processor pipeline before instruction execution and having a two-pipeline stage delay from generation in the second pipeline stage to receipt in the first pipeline stage, wherein the processor pipeline is to execute one or more instructions of the first thread while preparing to switch to the second thread without a processor stall and store results of the one or more instructions in a destination storage.

Claim 18 (original) The apparatus of claim 17, wherein the feedback signal is coupled between an instruction decoder and an instruction fetch unit.

Claim 19 (original) The apparatus of claim 18, wherein the instruction decoder is coupled to provide the feedback signal to the instruction fetch unit when a predetermined condition occurs.

Claim 20 (original) The apparatus of claim 19, wherein the instruction decoder includes logic to determine when the predetermined condition occurs.

Claim 21 (currently amended) The apparatus of claim 19, wherein the instruction decoder includes a lookup table to store a list of predetermined conditions to which an

instruction is compared and to generate the feedback signal when the instruction hits in the lookup table.

Claim 22 (currently amended) A system comprising:

a processor having a processor pipeline including a plurality of pipeline stages to receive and execute instructions, the processor pipeline including an instruction decoder and an instruction fetch unit, the processor pipeline having a feedback loop coupled to provide a feedback signal generated in the instruction decoder to the instruction fetch unit to cause the processor pipeline to switch from a first thread to a second thread, the feedback signal to originate from a location in the processor pipeline before instruction execution and having a two-pipeline stage delay from generation in the instruction decoder to receipt in the instruction fetch unit, wherein the processor pipeline is to execute one or more instructions of the first thread while preparing to switch to the second thread without a processor stall and store results of the one or more instructions in a destination storage;

a first bus coupled between the processor and a bus interface; and

a wireless interface coupled to the ~~processor pipeline~~ bus interface via a second bus and to provide an interface between an antenna and the processor.

Claim 23 (original) The system of claim 22, further comprising at least one storage device to store code to enable the processor pipeline to switch from the first thread to the second thread if a predetermined condition occurs during execution of the first thread.

Claim 24 (currently amended) The system of claim 23, wherein the at least one storage device includes code to enable the processor pipeline to execute the ~~at least~~ one or more instructions of ~~additional instruction in~~ the first thread while the system prepares to switch to the second thread.

Claim 25 (canceled)

Claim 26 (previously presented) The system of claim 22, wherein the instruction decoder is coupled to provide the feedback signal to the instruction fetch unit when a predetermined condition occurs.

Claim 27 (original) The system of claim 26, wherein the instruction decoder includes logic to determine when the predetermined condition occurs.

Claim 28 (previously presented) The system of claim 26, wherein the instruction decoder includes a lookup table that includes a list of predetermined conditions to which an instruction is applied, the instruction decoder to provide the feedback signal to the instruction fetch unit if the instruction matches an entry in the lookup table.

Claim 29 (original) The system of claim 22, wherein the wireless interface comprises a dipole antenna.

Claim 30 (currently amended) The method of claim [[4]] 1, wherein the predetermined conditions comprise instruction types.

Claim 31 (cancel)

Claim 32 (new): The method of claim 5, further comprising executing two instructions of the first thread while preparing to switch to the second thread, wherein the feedback signal has a two pipeline stage delay.